ABSTRACT OF THE DISCLOSURE

A 3D polysilicon ROM including an isolated SiO_2 layer on a silicon substrate, and an N+ polysilicon layer on the isolated SiO_2 layer. The N+ polysilicon layer is further defined by a plurality of parallel, separate word lines. A first oxide layer fills the space between the word lines. A dielectric layer is deposited on the word lines and the first oxide layer. A P- polysilicon layer is deposited on the dielectric layer and further defines a plurality of parallel, separate bit lines. The bit lines overlap the word lines, from a top view, to form an approximately cross shape. The neck structure may be individually formed between the P- and N+ polysilicon layers by wet etching the dielectric layer with dilute hydrofluoric acid. A second oxide layer fills the space between the bit lines and is on the word lines and the first oxide layer.